1126-94-374 **Robert Calderbank*** (robert.calderbank@duke.edu), Duke University, Durham, NC 27708, and **Georgios Mappouras**, **Daniel J Sorin** and **Alireza Vahid**. *Coding for Racetrack Memory.* Preliminary report.

Racetrack memory is a non-volatile memory engineered to provide both high density and low latency that is subject to synchronization or shift errors. This paper describes a very fast coding solution, in which "delimiter bits" assist in identifying the type of shift error, and easily implementable graph-based codes are used to correct the error, once identified. Previous proposals for handling shift errors in racetrack memory involved adding multiple read-write ports, and did not involve coding theory. (Received January 17, 2017)